



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/708,572	11/09/2000	Noriyuki Ito	1614.1093	2299

21171 7590 05/03/2004

STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER

SIEK, VUTHE

ART UNIT	PAPER NUMBER
----------	--------------

2825

DATE MAILED: 05/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

mx

Office Action Summary	Application No.	Applicant(s)	
	09/708,572	ITO ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 February 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,5 and 9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,5 and 9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to RCE application 09/708,572 and amendment filed on 8/26/2003. Claims 1, 5 and 9 remain pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1, 5 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishiyama et al. (U.S. Patent No. 5,519,630).

4. As to claims 1, 5 and 9, Nishiyama et al. teach the claim limitations of a computer program method for processing of hierarchically configured design data (at least in Figs. 18, 20, 23a-23b. col. 8, lines 24-48; col. 9, lines 38-49; col. 14, lines 17-54; col. 17, lines 8-67; col. 18, lines 1-50; col. 19, lines 52-67; col. 20, lines 1-8; lines 50-67; col. 21, lines 1-67; col. 22, lines 1-29) comprising a) obtaining first design data of a lower rank of hierarchy (information of design object or design data one-rank lower than the design object or design data); b) obtaining second design data of a rank of hierarchy higher than the lower rank of hierarchy, after the obtaining the first design data (a select rank of design object or design data or an upper-rank element, it is possible to retrieve all lower-rank elements forming such upper-rank element, where the lower-rank elements corresponding to retrieved first design data); and c) combining the second design data to the first design data. In addition, as claim 9, since Nishiyama teaches a method of

Art Unit: 2825

designing a hierarchical layout of a circuit (Figs. 17, 18, 20, 23), comprising receiving a designation of a lower rank from a user; retrieving design data the lower rank from a storage unit; retrieving wiring data of an upper rank from the storage unit, after the retrieving the design data; setting the wiring data in the design data; and displaying the design data in which the wiring data has been set on a display unit. The layout of a circuit includes wiring data of the rank structure as taught by Nishiyama. Displaying a hierarchical layout is inherently within the technological art of CAD tools as taught by Nishiyama.

Remarks

5. Applicants argued that Nishiyama only discusses selecting a lower rank at the same time as when an upper rank is selected. Examiner respectfully submits that Nishiyama teaches retrieving all lower-rank elements from each of the specified elements (col. 8, lines 35-40). Since information of all lower-rank elements are retrieved to each of the specified elements (an upper-rank elements), meaning that the upper-rank element is formed or obtained after the retrieving of the all lower-rank elements (first design data) or after the obtaining of the first design data. Accordingly, the current claims are not patentable over Nishiyama patent. Even if Nishiyama only discusses selecting a lower rank at the same time as when an upper rank is selected. Claiming obtaining an upper rank design data after obtaining design data of a lower rank is not patentable of the teaching of Nishiyama patent. This is because Nishiyama teaches storage unit for storing design data in a rank structure, therefore design data at any specified rank would be obtained from storage unit. In addition, Nishiyama teaches a

Art Unit: 2825

retrieving means for retrieving all lower-rank elements from storage unit, therefore an upper rank of design data would be obtained or design objects/design data for a desired circuit at a target level would be obtained. Therefore, designers can obtain circuit data (design data) on a desired level having a desired function, or verification results without special attention paid on the circuit data and the design procedures, merely by combining elements (design data) stored in the storage unit to carry out a function design and by specifying a design target serving as a target level (could be an upper level of hierarchy) (see at least col. 17-18). Per interpretation of the current claims, the disclosure of Nishiyama would be read into the claims. In addition, since Nishiyama suggested the designer can obtain circuit data on a desired level (in a rank structure) having a desired function, merely by combining elements stored in the library element memory mean to carry out a function design and by specifying a design target serving as a target level (col. 18, lines 35-41). There are stored only information relating to a design procedure and information relating to a rank structure and data of the design object are generated (col. 20, lines 25-33). Since the information of a rank structure is stored in memory, any level or rank of design data information can be retrieved or obtained and then combined. In addition, since design data of a rank structure are stored in memory, a designer can obtain or retrieve those design data whether lower-rank data is retrieved first and then higher-rank data is retrieved after or vice versa.

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Art Unit: 2825

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (703) 305-4958. The examiner can normally be reached on M-F (6:30-4:00) 2nd Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Vuthe Siek
April 26, 2004


VUTHE SIEK
PRIMARY EXAMINER